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EXAMINER	
ARNOLD, ADAM	

ART UNIT	PAPER NUMBER
2671	14

DATE MAILED: 06/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/739,956	PETHER ET AL.	
	Examiner	Art Unit	
	Adam Arnold	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11,13-21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11,13-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the receipt and entry of the applicant's amendment.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1, 4-11, 13-21 and 23-30 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Nowhere in the specification is there a description of a bus having a first address range and a second address range, where the X and Y registers are in the first range, and the memory is in a second range. Nor were these limitations in the original claims. The most detailed description of a bus connected to memory is at page 5, second paragraph, where: "The pixel pipeline 20 is connected to the system bus 16 by dedicated input and output data busses 22, 32 and has first and second X and Y registers 24, 26 which are each connected to the input data bus 22." This passage describes only a bus which can be used to transport data to memory. There is no delineation of different address ranges. Figures 2-5 also show a system bus connected to memory, but again there appears to be no disclosure of different address ranges within the memory.

Claim Objections

3. Claims 4-6 and 23-24 are objected to because of the following informalities: they depend from claims that have been cancelled. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-7, 20-21 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy, U.S. Patent No. 6,348,919. Referring to claim 1, Murphy discloses an apparatus for generating a region of graphics on a display (col. 1, line 13), the apparatus comprising: a range of addresses (Figure 5C and col. 7, lines 38-42, where a frame buffer memory is separate from a local buffer memory); a plurality of registers (col. 13, line 28) within an address range (col. 14, line 21) configured to store an x coordinate and a y coordinate of a pixel to be drawn (col. 14, lines 8-9); a memory directly connected to the bus (Figure 2E, which shows a FIFO memory directly connected to the PCI Bus); a calculation circuit configured to calculate an address for storage of data corresponding to the pixel in dependence on the x and y coordinates (col. 27, lines 1-14 and Figure 5C which shows a graphics pipeline calculating the local buffer address); a control circuit configured to control writing of said data in memory at said address (see Figure 5D and col. 62, line 7) by driving the address onto the bus (as pointed out below, a bus transfers data throughout the computer; as such, data must be driven onto the bus to be

usable); and a clipping circuit that serves to determine which coordinates fall outside of a particular threshold (col. 13, lines 39-41). Murphy does not explicitly disclose a bus having a first address range and a second address range. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a bus with a first address range and a second address range. One of ordinary skill in the art would have been motivated to do this because buses serve as conduits for data exchange within a computer system. Moreover, a memory address is broken up into different ranges. That is, each individual address or a group of addresses serve as a separate range from another address or group of addresses.

Referring to claim 4, Murphy does not explicitly disclose inhibiting writing of data to the address in response to the clipping circuit. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to inhibit writing of data to the address in response to the clipping circuit. One of ordinary skill in the art would have been motivated to do this because the purpose of a clipping circuit is to determine when pixel values are outside of a range, usually the viewing area. As such the values are extraneous and no further processing will be carried out on them.

Referring to claim 5, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 6, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 7, Murphy teaches a 1st register mapped to a 1st and 2nd location in memory and a 2nd register mapped to a 3rd and 4th location in memory (col. 13, lines 13-18 and 26-28, where each register is 32 bits, or 4 bytes, and each byte is a different location).

Referring to claim 20, Murphy discloses a system for generating a region of graphics on a display as described fully in claim 1 above. The remarks directed to claim 1 and 7 above, apply equally to claim 20. The apparatus of Murphy performing the steps is recited in the claim.

Referring to claim 21, the remarks presented above with respect to claim 4 apply equally to this claim.

Referring to claim 30, the remarks presented above with respect to claim 1 apply equally to this claim.

2. Claims 8-10 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Chiu, U.S. Patent No. 5,796,391. Referring to claim 8, Murphy discloses the graphics apparatus of claim 7. See 103 rejection above. Murphy does not teach an "address decoder" for monitoring the memory locations. Murphy does disclose monitoring the register's mapped addresses and subsequently writing the value and address tag to a FIFO buffer. Chiu teaches an address decoder attached to a control unit. See col. 3, line 45 and Figure 2, nos. 122 and 206. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have an address decoder for monitoring memory locations. One of ordinary skill in the art would have been motivated to do this because, as pointed by the applicant, the sole purpose of the address decoder is to "monitor each of the four address locations N to N+3 to see which is written to and apply an address location signal to the write control unit 36" (page 8, lines 3-5 of Applicant's Amendment). Although Murphy doesn't use the Chiu terminology, the functionality is the same as the applicant's.

Referring to claim 9, the remarks presented above with respect to claims 1 and 8 apply equally to this claim.

Referring to claim 10, the remarks presented above with respect to claims 1 and 8 apply equally to this claim.

Referring to claim 23, the remarks presented above with respect to claims 8 and 22 apply equally to this claim.

Referring to claim 24, the remarks presented above with respect to claims 8 and 22 apply equally to this claim.

3. Claims 11, 13, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Prouty, U.S. Patent No. 5,986,658. Murphy does not teach a style table for storing data corresponding to a predetermined style for the pixel, or a style counter for indexing the data in the style table. Prouty teaches a line style array for storing line style pattern features and a line style feature pixel counter. See Figure 2, elements 211 and 217. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table for storing data corresponding to a predetermined style for the pixel and a style counter for indexing the data in the style table. One of ordinary skill in the art would have been motivated to do this to provide for drawing complex line styles in real time. See Prouty, col. 1, lines 4-9. Further, both references are directed to the generation and use of raster computer graphics (see col. 9, lines 67 of Murphy and lines 1-2 of the Prouty abstract). Thus, Prouty simply provides details of the generation of a specific type of graphic, the type being more generally described and used by Murphy.

Referring to claim 13, Murphy does not teach a style table configured to store a non-repeating bit pattern up to a predetermined length. Prouty teaches an array large enough to handle line style pattern features. See Prouty, col. 7, line 29. At the time the invention was

made, it would have been obvious to a person of ordinary skill in the art to have a style table configured to store a non-repeating bit pattern up to a predetermined length. One of ordinary skill in the art would have been motivated to do this to provide for different size bit patterns.

Referring to claim 25, the remarks presented above with respect to claims 11 and 20 apply equally to this claim.

Referring to claim 26, Murphy does not disclose selecting a color for the pixel to be drawn dependent on the style data signal. Prouty discloses that in a preferred embodiment of their invention, the style array records color information for the line. See col. 5, line 19. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a style table record color information for the pixel. One of ordinary skill in the art would have been motivated to do this to record accurate information regarding the graphics display as well as the reasons above.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Prouty, further in view of Chiu. Referring to claim 14, the remarks presented above with respect to claims 8 and 11 apply equally to this claim.

5. Claim 15-19 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Ozcelik, Patent Publication No. 2002/0149626. Referring to claim 15, Murphy does not teach outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. Ozcelik teaches outputting a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. See paragraph 47. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to

output a word address corresponding to the address location in memory and a bit address representing a position of the pixel data within a word. One of ordinary skill in the art would have been motivated to do this to consume less storage space. See Ozcelik, paragraph 4. Further, Ozcelik provides the details of addressing memory for storage/retrieval of data such as done in Murphy.

Referring to claim 16, Murphy in view of Ozcelik discloses the graphics apparatus described in claim 15. See 103 rejection above. Murphy further discloses a second register for storing pixel data (col. 16, lines 15-16) and a multiplexer (or logic unit, i.e., a device for performing digital logical analysis) for writing data to a register (col. 5, line 33, where the register is memory mapped to an address space).

Referring to claim 17, Murphy in view of Ozcelik discloses the graphics apparatus described in claim 16. See 103 rejection above. Murphy does not explicitly disclose that the multiplexer combines data for two or more pixels. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have a multiplexer that combines data for two or more pixels. One of ordinary skill in the art would have been motivated to do this because the purpose of a multiplexer is to combine signals for transmission over a medium.

Referring to claim 18, Murphy in view of Ozcelik discloses the graphics apparatus described in claim 17. See 103 rejection above. Murphy discloses a comparator for comparing depth and color values (col. 75, line 57). Murphy does not disclose comparing addresses of pixels to be drawn. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to compare addresses of pixels. One of ordinary skill in the art would

have been motivated to do this because comparison operations are frequently used in graphics processing to preserve physical memory.

Referring to claim 19, Murphy discloses combining data for pixels where the values are different (col. 5, lines 60-65) and where the values are the same (col. 6, lines 2-4).

Referring to claim 27, the remarks directed to claims 17 and 20, above, apply equally to this claim.

Referring to claim 28, the remarks directed to claims 15 and 20, above, apply equally to this claim.

Referring to claim 29, the remarks directed to claims 18 and 20, above, apply equally to this claim.

Response to Arguments

6. Applicant's arguments have been considered although some are moot in view of new ground(s) of rejection. On page 14, second paragraph, the applicant asserts that Murphy is silent regarding a control circuit writing data in a memory across the bus. As pointed out in the arguments above, the bus is the means for transferring data in a computer system. Without it, there will be no data flow. Even though it was not explicitly shown in Figure 5C, it is inherent. Regarding a memory directly connected to the bus (third paragraph, page 14), the new grounds of rejection are given above. The applicant further contends Murphy is silent regarding a clipping circuit generating a signal. Murphy states (col. 13, lines 38-41) "Examples of control registers are the Scissor Clip unit min and max registers. Once initialized by the host, the chip only reads these registers to determine the scissor clip extents." The chip would only be able to

read these clipping registers if they generated a signal. Finally, the combination arguments on page 16 are moot in view of the new grounds of rejection.

Regarding the rejection to claim 15, the examiner agrees with the applicant that the motivation statement provided was insufficient and has provided an alternate statement above.

Regarding the rejection to claim 20, on bottom of page 17 the applicant contends Murphy is silent regarding a register memory mapped to two locations. Part of the quoted section states "Each register has an associated address tag, giving its offset from the base of the register file." This means that each register has an associated address a distinct distance from the base. Murphy discloses where each register is 32 bits, or 4 bytes, wide (col. 13, line 29) and since the registers reside on a 64 bit boundary, this is at least 2 locations. The applicant further points out a passage comprising a FIFO. The examiner does not agree with the applicant's interpretation of the passage, which states that "each write to a register causes the written value and the register's address tag to be written as a new entry in the FIFO." Nowhere does it state that the address passing stops at the FIFO. Moreover, this would still not obviate the disclosure shown above.

Regarding the rejection to claim 4, on page 19, the applicant traverses the assertion of inherency in inhibiting the writing of data to the address in response to the clipping circuit. The applicant cites a portion of Murphy, which discloses passing on a message when a depth test fails. These cases are distinct, in that the depth messages are passed on because "other units downstream need to keep their local DDA units in step." (See col. 8, lines 50-51). This situation regards a message describing the state of data, which can be used by other units. The clipping situation involves the data itself, which falls outside the system's constraints.

Regarding the rejection to claim 8, on page 20, the applicant contends that the Chiu address decoder receives an input signal rather than generating an output signal. The language of Chiu at column 3, line 45, appears to dispute this claim: "Address decoder 206 is a binary decoder which produces a load signal on one of four outputs..." Furthermore, the examiner's motivation statement above appears to be sufficient.

Regarding the rejection to claim 14, the examiner has corrected the grounds of rejection above.

Regarding the rejection to claim 16, the examiner has provided new grounds of rejection above.

Regarding the rejection to claim 19, the examiner has provided new grounds of rejection above.

In light of the new grounds of rejection, this action is Non-Final.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam Arnold whose telephone number is 703 305 8413. The examiner can normally be reached on Monday through Friday from 7:30 A.M. to 4:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman, can be reached on 703 305 9798. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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